



Phase Control Thyristor

DS5942-4 April 2013 (LN30255)

FEATURES

- Double Side Cooling
- High Surge Capability

KEY PARAMETERS

V _{DRM}	4200V
I _{T(AV)}	4500A
I _{TSM}	60800A
dV/dt*	2000V/µs
dl/dt	200A/µs

* Higher dV/dt selections available

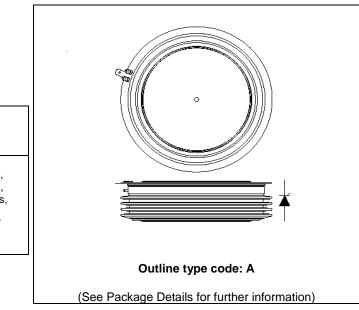


Fig. 1 Package outline

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V _{DRM} and V _{RRM} V	Conditions
DCR4500A42* DCR4500A40 DCR4500A36	4200 4000 3600	$\begin{array}{l} T_{vj} = -40^{\circ}C \ to \ 125^{\circ}C, \\ I_{DRM} = I_{RRM} = 300 mA, \\ V_{DRM}, \ V_{RRM} \ t_p = 10 ms, \\ V_{DSM} \ \& \ V_{RSM} = \\ V_{DRM} \ \& \ V_{RRM} \ + \ 100 V \\ respectively \end{array}$

Lower voltage grades available. *4100V @ -40° C, 4200V @ 0° C

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR4500A42

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.



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CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter Test Conditions		Max.	Units
Double Si	de Cooled			
I _{T(AV)}	Mean on-state current	Half wave resistive load		А
I _{T(RMS)}	RMS value	-	7068	А
Ι _Τ	Continuous (direct) on-state current	-	6330	А

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I _{TSM}	Surge (non-repetitive) on-state current	10ms half sine, $T_{case} = 125^{\circ}C$	60.8	kA
l ² t	I ² t for fusing	$V_R = 0$	18.48	MA ² s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Condition	Min.	Max.	Units	
R _{th(j-c)}	Thermal resistance – junction to case	Double side cooled	DC	-	0.00603	°C/W
		Single side cooled	Anode DC	-	0.01024	°C/W
			Cathode DC	-	0.01467	°C/W
R _{th(c-h)}	Thermal resistance – case to heatsink	Clamping force 83.0kN	Double side	-	0.001	°C/W
		(with mounting compound)	Single side	-	0.002	°C/W
T_{vj}	Virtual junction temperature	Blocking V _{DRM} / V _{RRM}		-	125	°C
T _{stg}	Storage temperature range			-55	125	°C
F _m	Clamping force			74.0	91.0	kN

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DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditio	Min.	Max.	Units	
I _{RRM} /I _{DRM}	Peak reverse and off-state current	At V _{RRM} /V _{DRM} , T _{case} = 125°C		-	300	mA
dV/dt	Max. linear rate of rise of off-state voltage	То 67% V _{DRM} , Т _ј = 125°С, ga	ate open	-	2000	V/µs
dl/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2x $I_{T(AV)}$	Repetitive 50Hz	-	200	A/µs
		Gate source 30V, 10Ω ,	Non-repetitive	-	500	A/µs
		t _r < 0.5µs, T _j = 125°C				
V _{T(TO)}	Threshold voltage – Low level	500 to 2200A at T _{case} = 125°	С	-	0.75	V
	Threshold voltage – High level	2200 to 8000A at T _{case} = 125	°C	-	0.92	V
г _т	On-state slope resistance – Low level	500A to 2200A at T _{case} = 125°C		-	0.205	mΩ
	On-state slope resistance – High level	2200A to 8000A at T _{case} = 125°C		-	0.122	mΩ
t _{gd}	Delay time	$V_D = 67\% V_{DRM}$, gate source 30V, 10 Ω		-	3	μs
		t _r = 0.5μs, T _j = 25°C				
tq	Turn-off time	$I_T = 5000A, T_j = 125^{\circ}C,$ $V_R = 200V, dI/dt = 5A/\mu s,$			900	μs
		dV _{DR} /dt = 20V/µs linear				
Qs	Stored charge	- I _T = 3000A, T _i = 125°C, dI/dt – 1A/μs,		2920	4875	μC
I _{RR}	Reverse recovery current	$V_{\text{Rpeak}} \sim 2500\text{V}, V_{\text{R}} \sim 1700\text{V}$		42	57	A
۱L	Latching current	$T_j = 25^{\circ}C, V_D = 5V$		-	3	A
IH	Holding current	$T_j = 25^{\circ}C, R_{G-K} = \infty, I_{TM} = 500$	0A, I _T = 5A	-	300	mA

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GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V _{GT}	Gate trigger voltage	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% V _{DRM} , T _{case} = 125°C	0.4	V
I _{GT}	Gate trigger current	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	400	mA
I _{GD}	Gate non-trigger current	At 50% V _{DRM} , T _{case} = 125°C	10	mA

CURVES

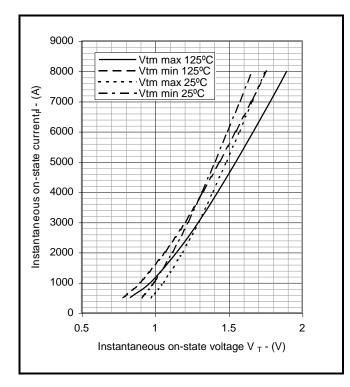


Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$$V_{TM} = A + Bln (I_T) + C.I_T + D.\sqrt{I_T}$$

Where A = -0.208640 B = 0.171688 C = 0.000113 D = -0.003842 these values are valid for T_j = 125°C for I_T 500A to 8000A



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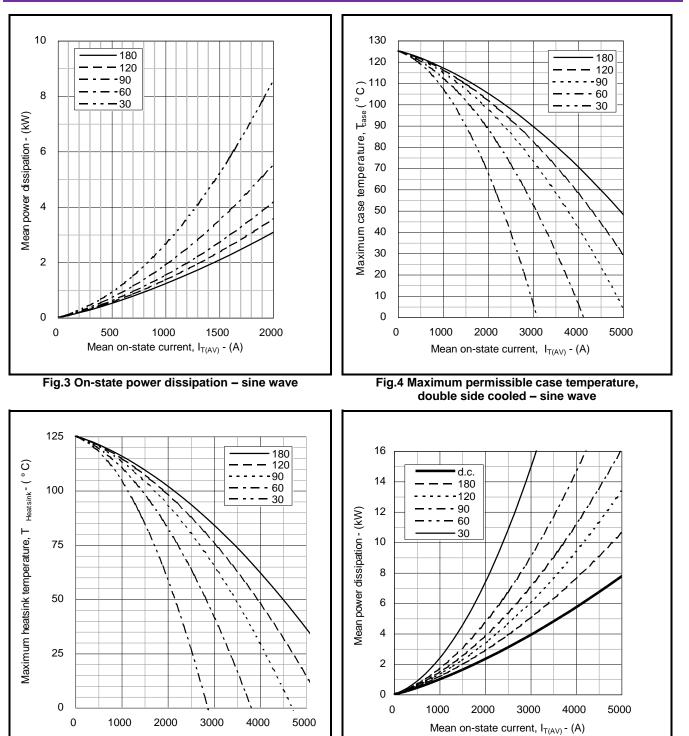


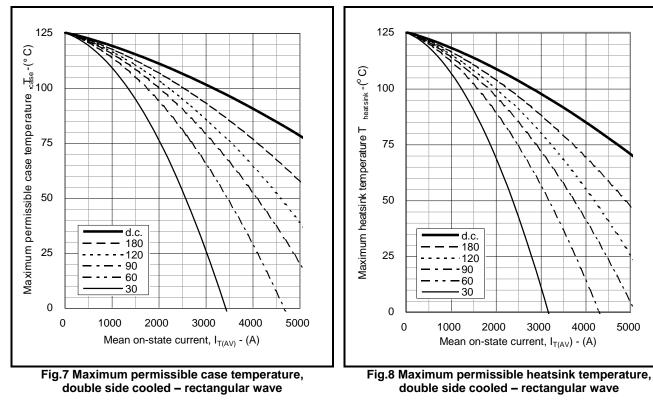
Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

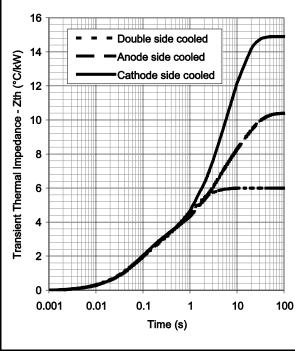
Mean on-state current, $I_{T(AV)}$ - (A)





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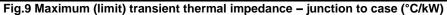
		1	2	3	4
Double side cooled	R _i (°C/kW)	3.01541	1.048955	0.983519	0.983519
Double Side Cooled	T _i (s)	0.703874	1.904794	0.059	0.059
Anode side cooled	R _i (°C/kW)	3.156003	4.092806	1.556555	1.623962
Anode side cooled	T _i (s)	2.69023	13.79162	0.059	0.205916
Cathode side cooled	R _i (°C/kW)	7.077369	3.483481	1.745839	2.634274
Callioue side cooled	T _i (s)	6.648601	8.436484	1.762119	0.08069

$$Z_{th} = \sum_{i=1}^{i=4} [R_i \times (1 - \exp(T/T_i))]$$

$\Delta R_{th(j-c)}$ Conduction

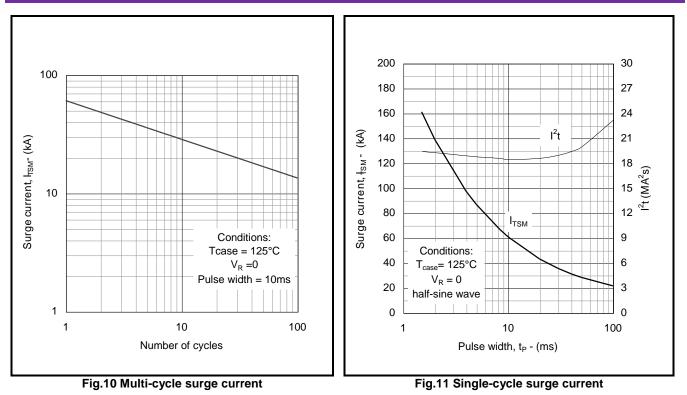
Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

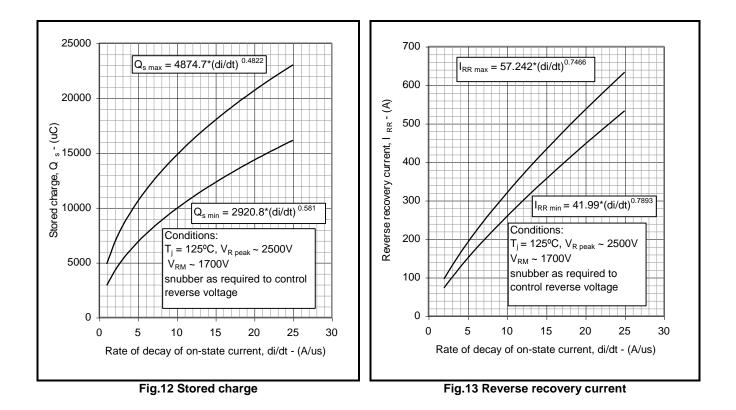
D	ouble side o	cooling	Ar	node Side	Cooling	Cathode Sided Coc		
	ΔZ_{th}	(z)		$\Delta Z_{th}(z)$			ΔZ	_{th} (z)
θ°	sine.	rect.	θ°	sine.	rect.	θ°	sine.	rect.
180	0.44	0.31	180	0.42	0.30	180	0.42	0.30
120	0.49	0.43	120	0.47	0.41	120	0.47	0.41
90	0.55	0.49	90	0.52	0.46	90	0.52	0.46
60	0.60	0.55	60	0.57	0.52	60	0.57	0.52
30	0.64	0.61	30	0.61	0.58	30	0.60	0.58
15	0.66	0.64	15	0.62	0.61	15	0.62	0.60





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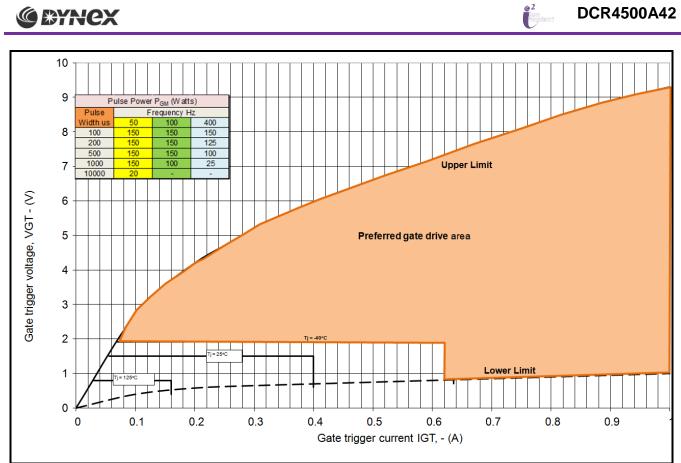


Fig14 Gate Characteristics

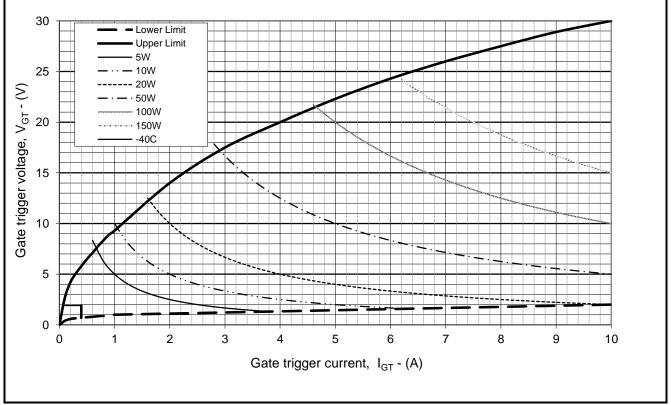


Fig. 15 Gate characteristics



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PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

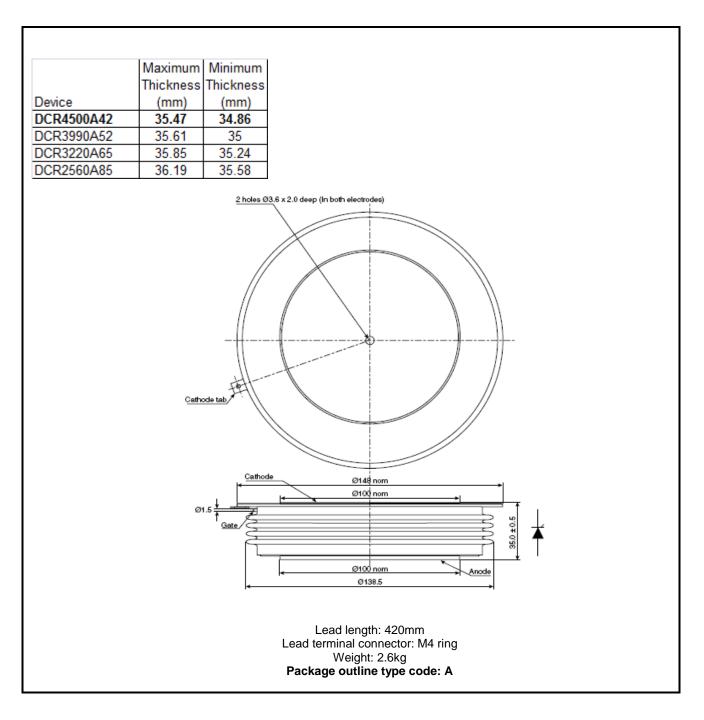


Fig.16 Package outline



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